REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested.

Claims 1-19 are pending within this application. No claims are amended herein. No claims are newly added herein. No claims have been allowed.

Continued Examination Under 37 C.F.R. 1.144

Applicant appreciates the Examiner's withdrawal of finality of the previous office action and the entry of applicant's submission filed on 10 March 2003.

However, insofar as the Examiner accurately notes that applicant's submission filed 10 March 2003 was a request for continued examination, rather than a continuing application or a substitute application, applicant asserts that the present office action may apparently not properly be made FINAL. MPEP 706.07(b) & (h).

Thus, applicant respectfully requests that the finality of the present office action also be withdrawn.

Double Patenting

The Examiner has advised that if claims 14-19 are found allowable, claims 2-7 would be objected to under 37 C.F.R. 1.75 as being a substantial duplicate thereof.

Applicant notes that while the Examiner accurately advises that claims 2-7 and 14-19 are substantial duplicates [in their wording], each of claims 2-7 is dependent upon

independent claim 1 and each of claims 14-19 is dependent upon independent claim 13. Applicant further notes that the Examiner does not apparently advise that independent claim 13 is a substantial duplicate of independent claim 1. Thus, since dependent claims carry all of the limitations of independent claims from which they depend, and since the Examiner apparently implicitly acknowledges that independent claim 1 and independent claim 13 are not substantial duplicates, applicant asserts that claims 2-7 and 14-19 may not properly be regarded as substantial duplicates when integrating the limitations of the independent base claims from which they depend. Thus, applicant asserts that claims 2-7 may not properly be objected to under 37 C.F.R. 1.75 as substantial duplicates of claims 14-19, if claims 14-19 are found allowable.

Claim Rejections - 35 U.S.C. § 112

The Examiner has rejected claim 13 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In connection with the foregoing rejection, the Examiner asserts that the specification as originally filed fails to provide support for applicant's limitation of "supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer" since the supplemental thermal annealing would inherently produce another gate dielectric layer since it is equivalent to the twice thermally oxidized substrate of the prior art.

In response, applicant directs the Examiner's attention to paragraph 0056 (counted by hand) which provides that applicant's compensating thermal annealing environment 40 (in accord with applicant's Fig. 7) may comprise a purely thermal annealing environment

(i.e., an unreactive environment). Since applicant's supplemental thermal annealing environment 40 may comprise a purely thermal annealing environment, it is thus clearly not inherent within applicant's invention that applicant's supplemental thermal annealing would produce another gate dielectric layer upon applicant's thermally compensated once thermally oxidized semiconductor substrate 30'' as illustrated in Fig. 7. In addition, applicant also notes that applicant's once thermally oxidized semiconductor substrate 30' as illustrated in Fig. 6 is fully populated with a series of gate dielectric layers 34a, 34b and 34c upon a series of active regions 31a, 31b and 31c thereof prior to being exposed to applicant's compensating thermal annealing environment 40 when forming applicant's thermally compensated once thermally oxidized semiconductor substrate 30''. For this reason also, incident to forming applicant's thermally compensated once thermally oxidized semiconductor substrate 30'' from applicant's once thermally oxidized semiconductor substrate 30' another gate dielectric layer is not formed upon applicant's thermally compensated once thermally oxidized semiconductor substrate 30'' since applicant's invention as disclosed within Figs. 6-7 provides no apparent location for the same.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejection of applicant's claim 13 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1-2, 7-8, 12, 14 and 19 for reasons of record (within an office action mailed 24 September 2002) as directed towards rejection of applicant's claims 1-2, 7-8 and 12 under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

In response, applicant respectfully disagrees within the Examiner's reading of applicant's admitted prior art insofar as the Examiner within the paragraph bridging pages 2-3 of the office action mailed on 24 September 2002 characterizes applicant's thermal oxidizing process step 24 in applicant's Fig. 5 as a supplemental thermal annealing process step in accord with applicant's claim 1, clause 3 and applicant's claim 8, clause 3.

Rather, applicant's thermal oxidizing process step 24 in applicant's Fig. 5 is employed for forming applicant's third gate oxide layer 22 upon applicant's active region 11c of applicant's three times thermally oxidized semiconductor substrate 10"' (page 19, second full paragraph), and is thus not a supplemental thermal annealing process step but rather a non-supplemental thermal oxidizing process step which is employed for forming a specific gate dielectric layer of a specific thickness upon a specific active region of applicant's semiconductor substrate Within applicant's admitted prior art as illustrated in Fig. 1 to Fig. 5 and as cited by the Examiner, applicant's thermal oxidizing process steps 16, 20 and 24 are employed for forming applicant's corresponding gate dielectric layers 14a, 18a and 22 upon applicant's corresponding active regions 11a, 11b and 11c of applicant's three times thermally oxidized semiconductor substrate 10"', and thus there is no supplemental thermal annealing process step employed within applicant's admitted prior art.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within applicant's admitted prior art, in particular with respect to a supplemental thermal annealing process step for thermally annealing a semiconductor substrate to compensate for forming thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps, applicant asserts that claim 1 and claim 8 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

Since remaining claims within this rejection which are dependent upon claim 1 or claim 8 carry all of the limitations of claim 1 or claim 8, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art. Patentability of claims 14 and 19 is predicated upon their dependence upon claim 13.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 1-2, 7-8, 12, 14 and 19 under 35 U.S.C. § 102(b) be withdrawn.

Claim Rejections -- 35 U.S.C. § 103

The Examiner has rejected claims 3-6, 9-11, 13 and 15-18 for reasons of record (within the office action mailed on 24 September 2002) as directed towards rejection of claims 3-6 and 9-11 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art.

While not precluding the existence of independent patentable distinctions between: (1) applicant's admitted prior art; and (2) that which is claimed within claims 3-6 and 9-11, applicant predicates patentability of applicant's claims 3-6 and 9-11 upon their dependence upon applicant's claim 1 or claim 8.

In addition, with regard to claims 13 and 15-18, beyond the above discussion with respect to claim 1 and claim 8 (which also applies to claim 13) applicant notes that claim 13 contains therein additional subject matter directed towards employing a supplemental thermal annealing process step for a semiconductor substrate, absent forming a gate dielectric layer upon the semiconductor substrate, such as to provide within claim 13 additional limitations which are neither disclosed nor claimed within applicant's admitted prior art. Thus, applicant asserts that

claim 13 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art.

Since claims 15-18 are dependent upon claim 13 and carry all of the limitations of claim 13, applicant additionally asserts that claims 15-18 may also not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejections of applicant's claims 3-6, 9-11, 13 and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art be withdrawn.

Other Considerations

Applicant again acknowledges the prior art of record cited by the Examiner, but not employed in rejecting applicant's claims to applicant's invention, including: (1) Su et al. (U.S. Patent No. 5,576,573); (2) Gardner et al. (U.S. Patent No. 6,054,374); (3) Jenq (U.S. Patent No. 6,303,521); (4) Pearce et al. (U.S. Patent No. 6,358,865); and (5) Mukhopadhyay et al. (U.S. Patent No. 6,399,488), as generally pertinent to applicant's invention.

No fee is due as a result of this response.

SUMMARY

Applicant's invention as disclosed and claimed within claim 1 and claim 8 is directed towards a method for fabricating a semiconductor substrate to form thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered

plurality of thermal oxidation process steps. The method employs a supplemental thermal annealing process step, which is absent from applicant's admitted prior art, to compensate for the less than corresponding maximum numbered plurality of thermal oxidation process steps. In addition, and in accord with claim 13, the supplemental thermal annealing process step does not form a gate dielectric layer upon applicant's semiconductor substrate.

CONCLUSION

On the basis of the above remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

Randy W. Tung (Reg. No. 31,311)

838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302
248-540-4040 (voice)
248-540-4035 (facsimile)

TUNG & ASSOCIATES
Intellectual Property Law

Date: May 23, 2003

TO: **Examiner Richard A. Booth** **(703) 872-9319**
Art Unit: 2812

FAX Operator: Kathy Dixon

FAX Number: (248) 540-4035

Telephone Number: (248) 540-4040

Subject Matter: 09/ 920,911 Attorney Doc: 67,200-506

Message:

Total number of pages sent: - **13** - **(including this cover sheet)**

838 West Long Lake Rd. • Suite 120 • Bloomfield Hills, MI 48302 • (248) 540-4040 • Fax: (248) 540-4035